KA49702A
Application Notes

Battery Monitoring IC (BMIC)
for Industrial Application

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Chapter 1 Overview

1.1 Description

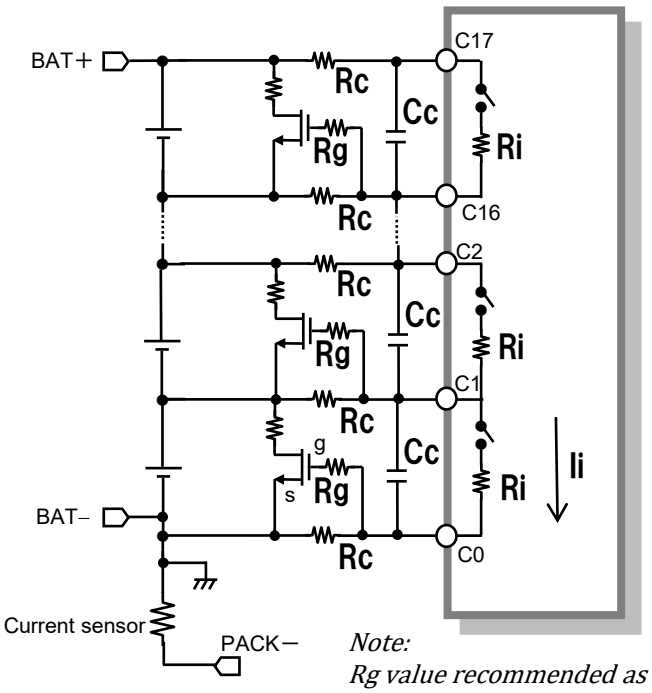
This is the application note for using KA49702A, which is a battery monitoring IC with protection function.

All the materials in this application notes are provided as design references only and not mass production guaranteed.

Sufficient evaluation and verification is required prior to mass production.

Chapter 2 Input RC and components setting for Cell Balance operation

2.1 RC external Cell Balancing



Note:
Rg value recommended as 1kohm for hotplug solution

Fig. 2.1.1 Parameter for external cell balance

1) *Calculate Rc*

$$Vgs = \frac{Vcell * Rc}{2Rc + Ri} \qquad Ri = 20ohm$$

$Vgs \geq Vth(in\ order\ to\ turn\ on\ FET)$

$Suppose\ Vth = 1.5V$ Vcell = 3.7V

$$Rc \geq Ri * \frac{Vth}{Vcell - 2Vth} = 43ohm$$

$and\ Rc < 5kohm\ (for\ input\ impedance\ limitation)$

$Rc = 1kohm{\sim}4kohm\ is\ recommended$

2) *Calculate Cc*

$$fc = \frac{1}{2\pi * 2Rc * Cc} \leq \frac{fs}{2}$$

$fc\ depends\ on\ the\ sampling\ time\ of\ our\ system$

$$\left(MAX(fc) = \left(\frac{fs}{2}\right) = \frac{1}{50us * 2} = 10kHz\right)$$

$eg.when\ fs = 20kHz, Rc = 1kohm$

$$Cc \geq \frac{1}{fs * \pi * 2Rc} = 0.008\text{uF}$$

$Using\ 10 * Cc\ \ is\ recommended$

2.2 RC internal Cell Balancing

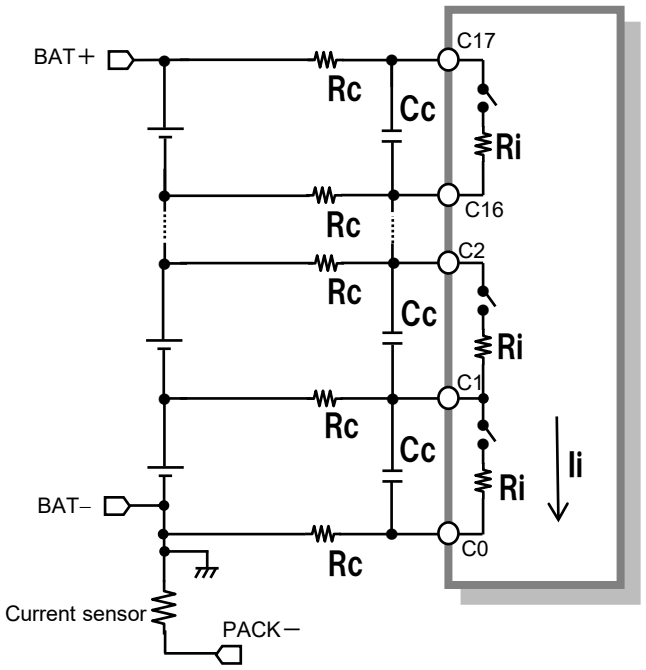


Fig. 2.2.1 Parameter for internal cell balance

1) *Calculate Rc*

$$Ii = \frac{Vcell}{2Rc + Ri}$$

$Ii\ depends\ on\ the\ design\ target\ of\ your\ system$
$(Max(Ii) = 50mA)$

$Suppose\ Vcell = 4.2V\ \ Ii = 50\text{mA}$

$$Rc \geq \frac{1}{2} * \left(\frac{Vcell}{Ii} - Ri\right) = 32ohm$$

2) *Calculate Cc*

$$fc = \frac{1}{2\pi * 2Rc * Cc} \leq \frac{fs}{2}$$

$fc\ depends\ on\ the\ sampling\ time\ of\ our\ system$
$(MAX(fc) = \left(\frac{fs}{2}\right) = \frac{1}{50us*2} = 10kHz)$

$eg.when\ fs = 20kHz, Rc = 40ohm$

$$Cc \geq \frac{1}{fs * \pi * 2Rc} = 0.2\text{uF}$$

$Using\ 10 * Cc\ \ is\ recommended$

Chapter 2 Input RC and components setting for Cell Balance operation

2.3 NMOS for external cell balancing

When applying VBAT, high voltage may occur transiently between the external FET pins for cell balance because normally there is RC filter at VBAT line.

External Cell balance FET with high voltage tolerance is highly recommended to withstand this transient spike.

In case high voltage tolerance FET cannot be used in the system, user can consider to separate VBAT from C17 as shown in Fig.2.3.2.

Battery cells connection sequence is documented on page 20

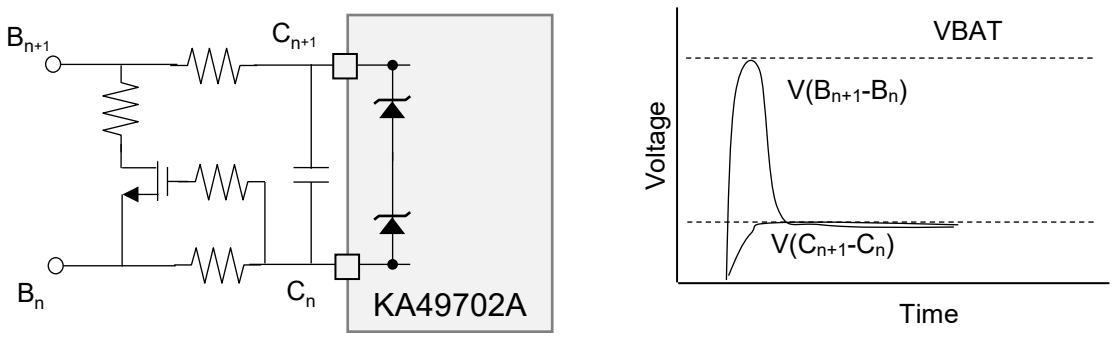


Fig. 2.3.1 Transient High Voltage

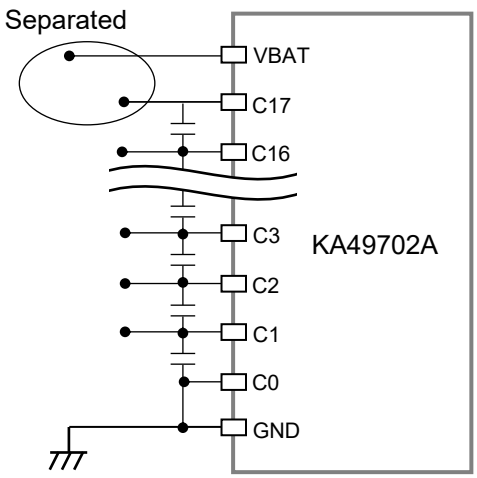


Fig. 2.3.2 Separated VBAT

Chapter 2 Input RC and components setting for Cell Balance operation

2.4 BJT for external cell balancing

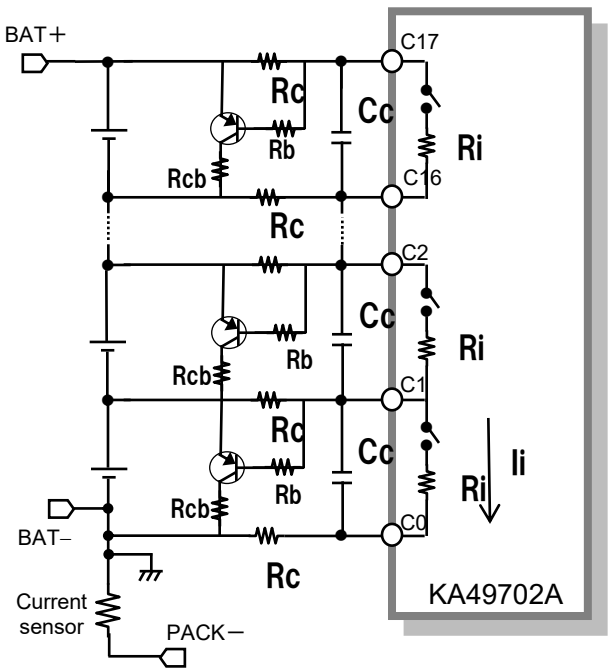


Fig. 2.4.1 Cell balance PNP

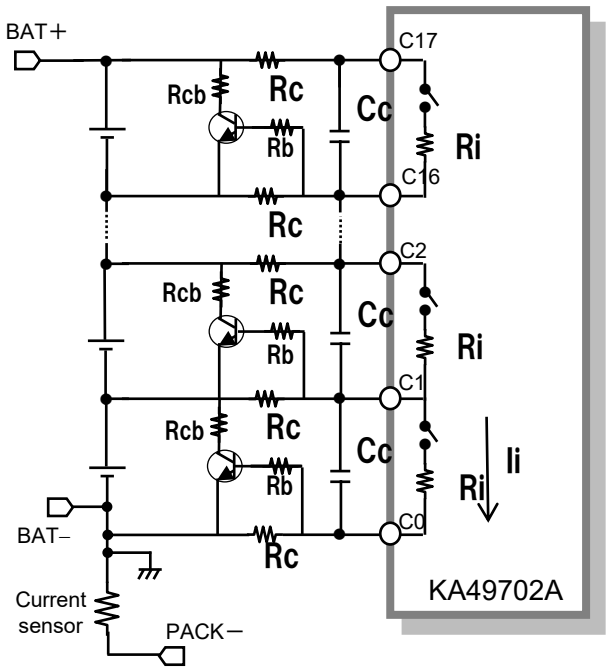


Fig. 2.4.2 Cell balance NPN

Example for parameter selection :

Rc=1kohm, Rcb =75ohm, Rb=100ohm

PNP BJT BC856 (Veb = 0.8V, Vce(sat)= -0.1V)

Icb = (Vcell - Vce(sat)) / Rcb = 48mA when Vcell = 3.7V

Chapter 3 High-Side Switch and Charge Pump components setting

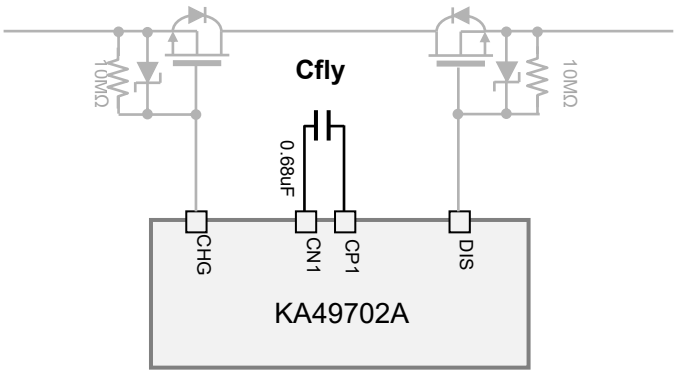
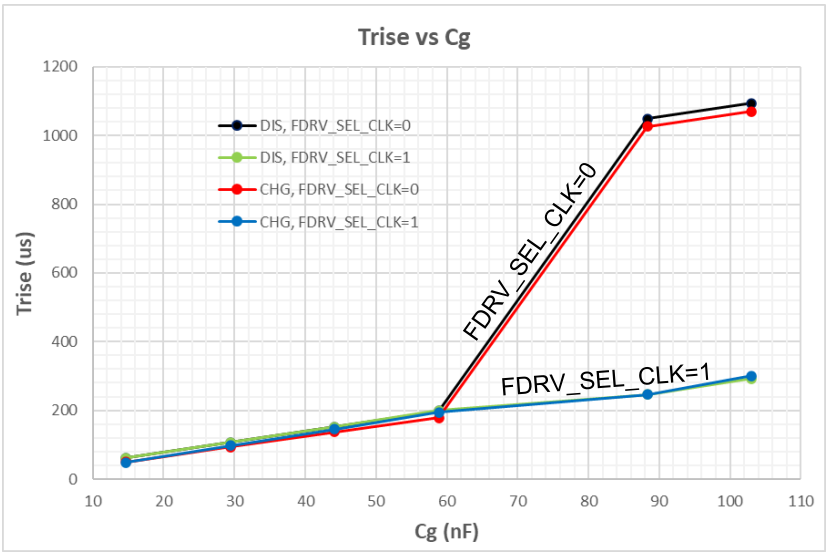


Fig. 3.0 Flying Capacitor & FET Gate Capacitance

Flying capacitor (Cfly) is the capacitor connected across CP1/CN1.
The voltage across this capacitor is charged to 11V(typ) internally. FET Gate capacitance (Cg) is the total capacitance at the gate terminal of the external NFET switch. During operation, charge from Cfly is transferred to Cg periodically to turn on the external NFET switch. The value of Cfly & Cg will affect both FET driver turn on rise time (Trise) & turn off fall time (Tfall).

3.1 Cg affecting FET Driver Rise Time

The internal charge pump is operating with a default clock of 2kHz. In application when large Cg is used, the FET driver turn on rise time might be longer than the clock period. The internal clock frequency can be slowed down to 500Hz, by setting FDRV_SEL_CLK (0x04[11]) to “1”.
Fig 3.1.1 shows the FET driver turn on rise time versus Cg capacitance when FDRV_SEL_CLK=1/0. This register function should be set before turning on the FET. After the FET is turned on, reset the charge pump to operate at default 2kHz.



Note:
Cfly = 3.3uF,
Trise = 10% to 90% delay
Data on left is taken with CHG FET turning ON before DIS FET

Fig. 3.1.1 FET Driver Rise Time

Chapter 3 High-Side Switch and Charge Pump components setting

3.2 Cg affecting FET Driver Fall time

Fig 3.2.1 shows FET Driver Fall Time versus Cg.
As Cg increases, longer fall time is expected to turn OFF the FET

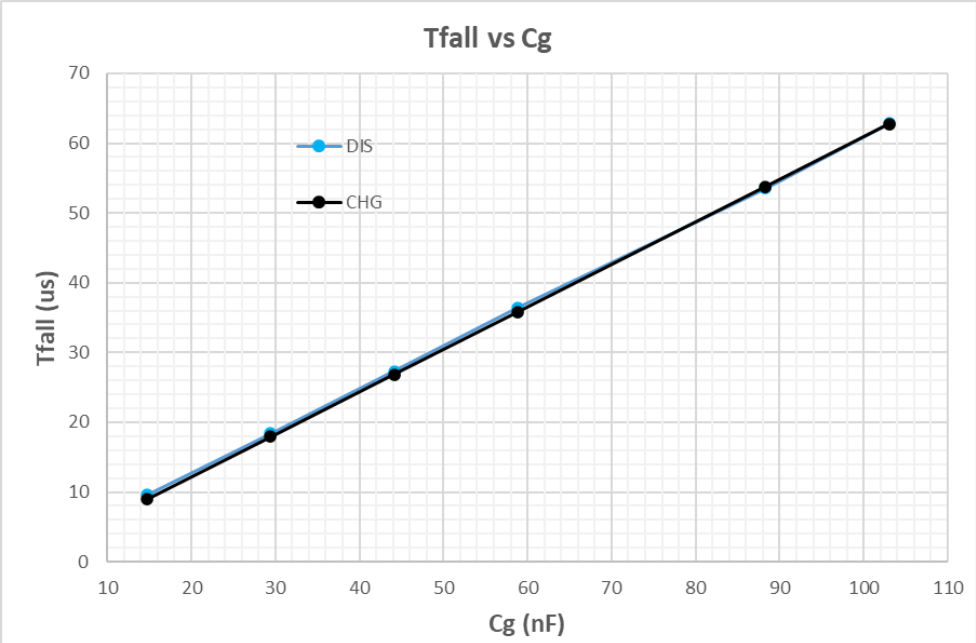


Fig. 3.2.1 FET Driver Fall Time

Note : Cfly = 3.3uF, Tfall = 90% to 10% delay

Chapter 3 High-Side Switch and Charge Pump components setting

3.3 Cfly affecting FET Driver Rise time

The Cfly capacitor charge is shared between DIS and CHG FET.

During both FETs 1st turn on, a portion of Cfly charge is transferred to Cg resulting in a transient voltage drop.

If this drop is more than 10%, Trise will take more than 1 charge pump clock cycle to reach 90% of its steady state.

Fig 3.3.1 shows FET Driver Rise Time versus Cfly.

In this setup DIS is turned on before CHG, hence CHG will have larger transient voltage drop as compared to DIS at first turn on.

When Cfly is not sufficiently larger than Cg, FET turn on rise time increases

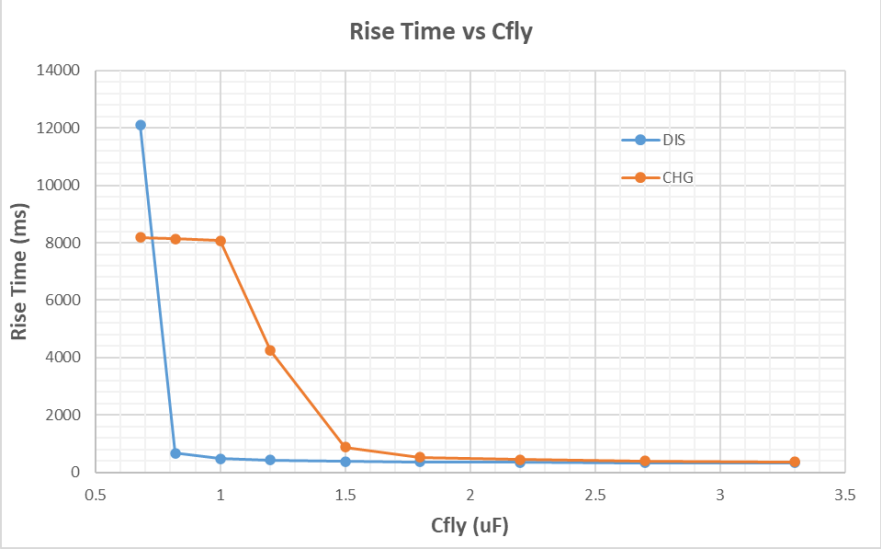


Fig. 3.3.1 FET Driver Rise Time

Note : Cg = 100nF, Trise = 10% to 90% delay, FDRV_CLK_SEL = 1

Chapter 3 High-Side Switch and Charge Pump components setting

3.4 Effective FET gate capacitance (Cg) estimation

Fig 3.4.1 shows a typical VGS vs Qg graphs in a FET specification.
In this example, the FET has the following characteristics :

1) At V_{DD}=50V and I_D=180A,
2) ~175nC need to be discharge to get Vgs back from 10V to 0V,
3) Hence, the effective Cg = Qg/Vgs =17.5nF.

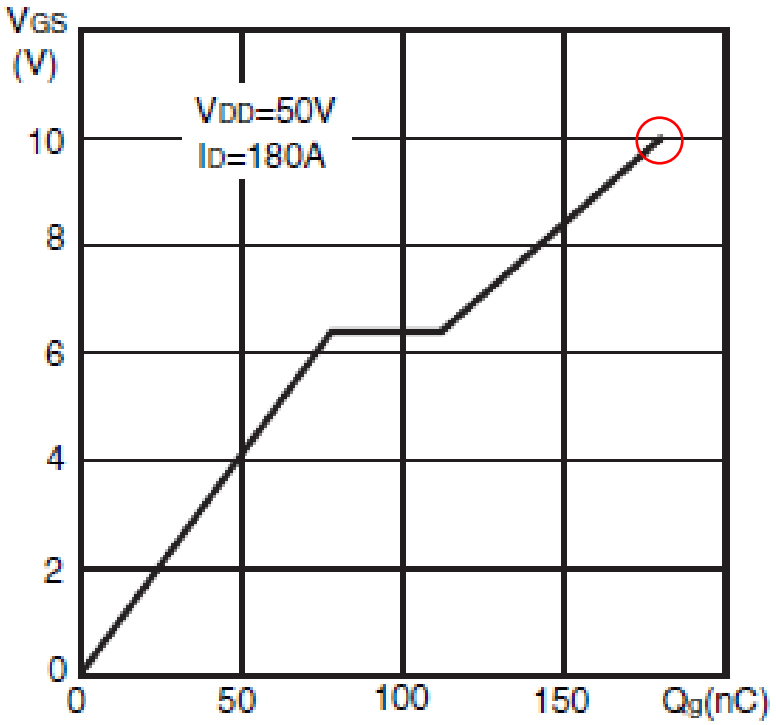


Fig. 3.4.1 Gate charge vs gate-source voltage

Note:
When using power MOS FET in parallel, it is recommended to insert resistor around 50-100ohm (tuned the value by evaluation) between each gate of FET.
This may reduce abnormal voltage vibration during high current on off operation.

Chapter 4 Regulators Components and setting

4.1 VDD50 RC and BJT components

VDD50 BJT and RC devices must be connected as shown in Fig. 4.1.1.

C_{REGB}, R_{REGB}, C_{VDD50}, R_{VDD50} should be selected according to the loop characteristic of the regulator design with the select NPN BJT. The recommended RC values with the accompany BJT devices are shown in Table. 4.1.2 below. These devices are to be used together with the recommended NPN BJT to ensure the best stability and load transient performance for VDD50 regulator. In case NPN BJT is changed from the recommended list, it is necessary to perform enough evaluation check and optimize the RC value again.

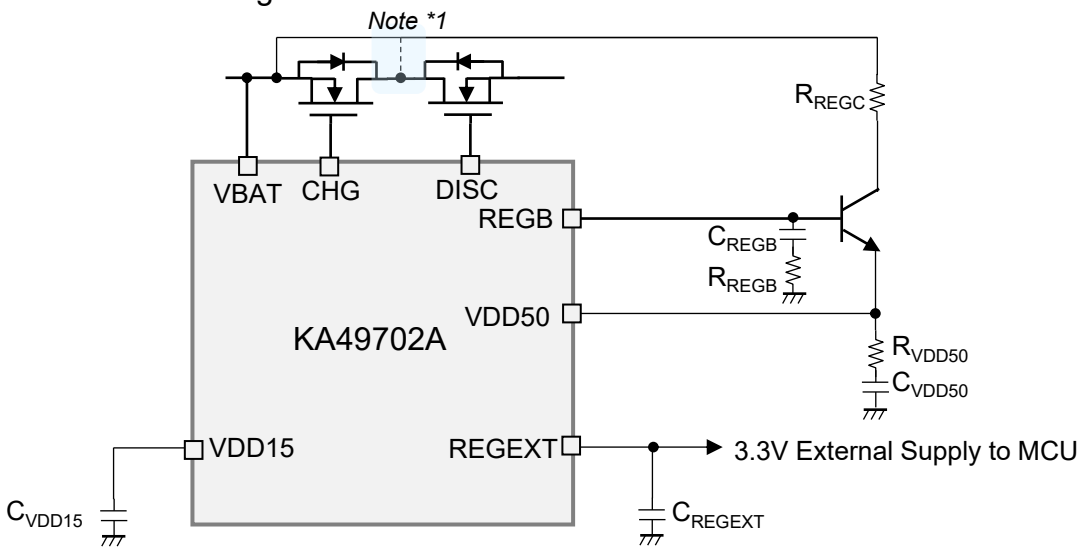


Fig. 4.1.1 VDD50 circuit

Note :
*1 : Default connection of VDD50 NPN's collector supply is to VBAT pin. Do note that connection to center point of CHG and DISC FET is also possible if supply source need to come from either VBAT or VPACK.

NPN / Component	Recommended Component Value	Remark
	FZT458TA PZTA42T	
C_{REGB}	0.1uF	<±50% for stability.
R_{REGB}	10kΩ	
C_{VDD50}	10uF	<±30% for stability.
R_{VDD50}	0.33Ω	
R_{REGC}	400Ω	Min VBAT > 30V for 50mA max load condition. Choose resistor with suitable power dissipation ability.
C_{REGEXT}	1uF	
C_{VDD15}	2.2uF	
C_{VDD50} / (C_{REGEXT}) Ratio	> 5	Meet ratio requirement in tolerance condition.

Table. 4.1.2 Recommended BOM for VDD50 regulator

Chapter 4 Regulators Components and setting

VDD50 BJT and RC devices must be connected as shown in Fig. 4.1.1.

When selecting the NPN BJT, it is recommended to consider the following key factor as listed in Table. 4.1.3 below. Recommended BJT are listed in Table. 4.1.2.

BJT Parameters	Minimum	Maximum	Notes.
DC current gain (h_{FE})	Depends on output current needed	Depends on stability of regulator.	$h_{FE} = I_C / I_B$ (I_B is base current from REGB pin. I_C is output collector current.) Do ensure to use NPN beta > 40
Continuous collector current (I_C)	Internal IC loading (2mA) + REGEXT loading needed (max 50mA)	Depend on NPN current rating as well as thermal performance	REGEXT can be used as power supply for external circuit. OCP of REGEXT is up to 100mA. Do ensure to use NPN beta > 40 to keep $I_{VDD55} > I_{REGEXT}$
Collector emitter voltage (V_{CEO})	> Charger input or >$VBAT_{max}$ with sufficient margin	--	Maximum battery level $VBAT_{max}$ or charger input voltage will be seen at V_{CE} of the NPN. It is necessary for selected NPN to be able to withstand this voltage applied to it with sufficient margin being considered.
Thermal	$Tj = (Pd \times \theta_{j-a}) + Ta$	--	(1) Tj ≦Tjmax BJT; (2) θ_{j-a} : Junction to ambient thermal Coefficient (It is recommended to have enough evaluation with the final PCB to determine actual θ_{j-a} and Tj of the NPN) (3) Ta=Ambient Temperature (4) Pd= ($VBAT_{max}$-5.0V) x I_{Cmax}

Table. 4.1.3 VDD50 BJT selection consideration

Chapter 4 Regulators Components and setting

4.2 REGEXT settings

REGEXT is a supply for external MCU and the internal interface I/O pins (ALARM1, FETOFF1, SPI, GPIO3, GPIO4. It takes the input voltage from VDD50 and generates a regulated 3.3V as shown in Fig. 4.2.1. Besides providing power for the interface I/O pins for internal usage, this REGEXT can support an external max load of 50mA for the MCU. The recommended components are shown in Table 4.2.3.

For MCU that uses 5V supply, VDD50 can be connected to REGEXT directly as shown in Fig. 4.2.2. Turn OFF REGEXT function by setting REGEXT_EN register to be “0”(address 0x02h[8]=“0’) The C_{REGEXT} is not needed in the 5V mode but do ensure VDD50 output cap is near to REGEXT routing in PCB layout to enhance transient response at REGEXT output. The recommended components are shown in Table 4.2.3.

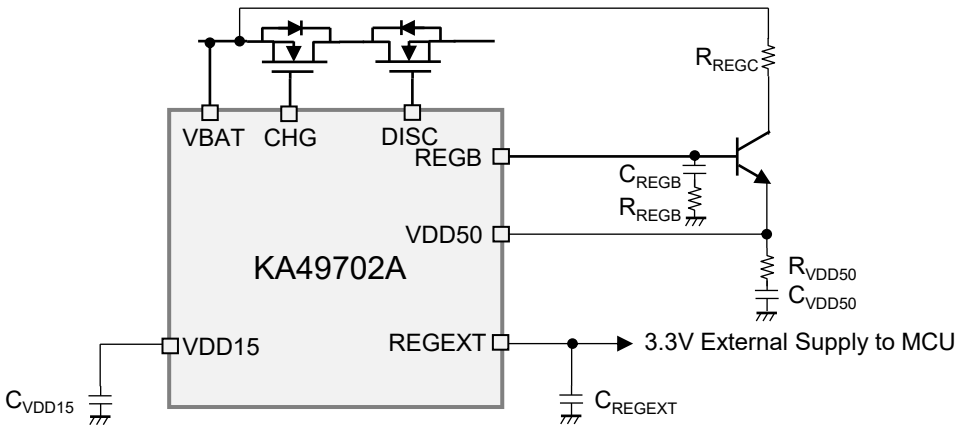


Fig. 4.2.1 REGEXT circuit for 3.3V regulation mode

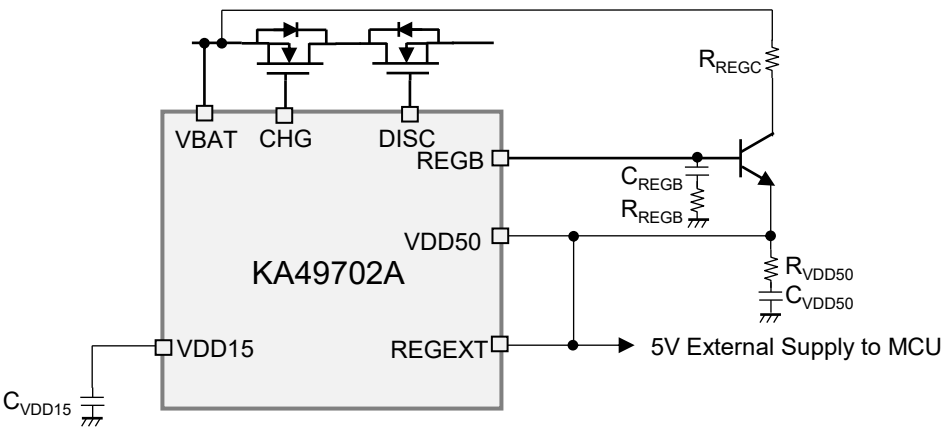


Fig. 4.2.2 REGEXT circuit for 5V mode

Component	Recommended Component Value		Remark
	3.3V REGEXT	5V REGEXT	
C_{REGEXT}	1uF	--	<±20% for stability.
C_{VDD15}	2.2uF	2.2uF	<±20% for stability.

Table. 4.2.3 Recommended BOM for REGEXT regulator

Chapter 4 Regulators Components and setting

4.3 Low current application

For low current application where REGEXT is not used as an external supply VDD50 can be connected to the REGB directly as shown in Fig. 4.3.1.

Fig. 4.3.2 shows the VDD50 low power mode setting for REGEXT=5V setting. The C_{REGEXT} is not needed in the 5V mode but do ensure VDD50 output cap is near to REGEXT routing in PCB layout to enhance transient response at REGEXT output

The recommended values for C_{VDD50}, C_{VDD15}, $C_{REGEXT,}$ R_{VDD15} are listed in Table. 4.3.3 for the proper startup of the system. Note that REGB can only supply 3.3mA current. Thus, VDD50 rise time can be up to 60ms. Please ensure that the VPC startup pulse is at least 100ms.

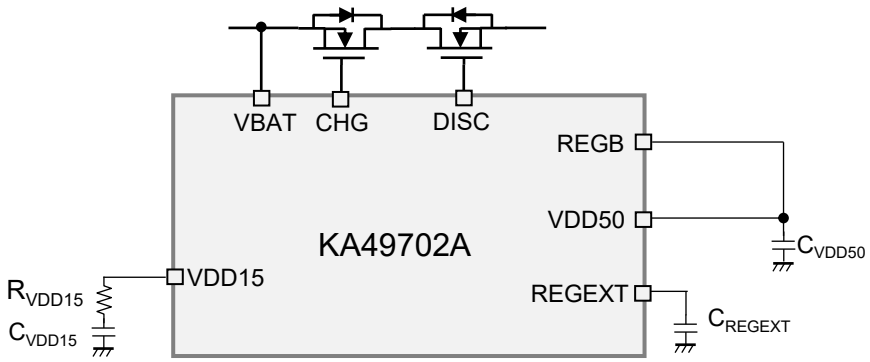


Fig. 4.3.1 VDD50 low power mode setting for REGEXT= 3.3V

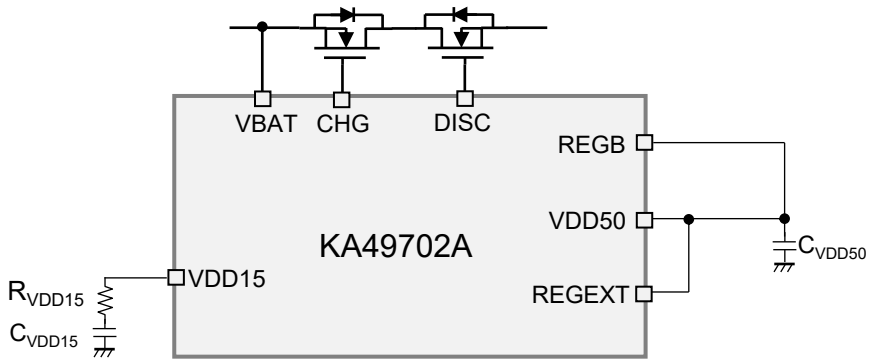


Fig. 4.3.2 VDD50 low power mode setting for REGEXT= 5V

Component	Recommended Component Value		Remark
	3.3V REGEXT	5V REGEXT	
C_{VDD50}	20uF	20uF	<±20% for stability.
C_{REGEXT}	1uF	--	<±20% for stability.
C_{VDD15}	1uF	1uF	<±20% for stability.
R_{VDD15}	1Ω	1Ω	

Table. 4.3.3 Recommended components for VDD50 Low Current Application

Chapter 5 Unused pins setting

5.1 Unused Cell Pins:

1) All unused Cell pins named 'NC' should be connected via resistor of the same input filter value to the cells. Refer to Fig 5.1.1
2) For lower cells count system, the unused battery cells pins (C3~C15) should be connected as shown in Fig 5.1.2 / 5.1.3 / 5.1.4
3) Fig.5.1.4 is an example for 4-cell solution, the cells can be added from lower to upper (C3,C4…) for the solution which need more cells.

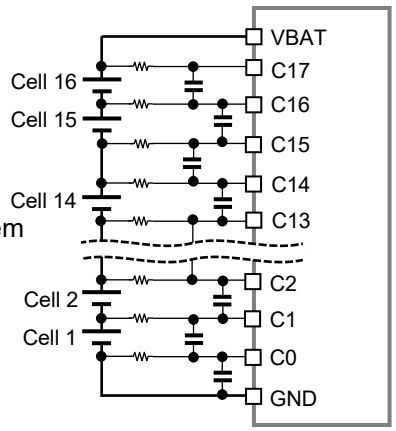


Fig. 5.1.1
Example of
16 Cell System

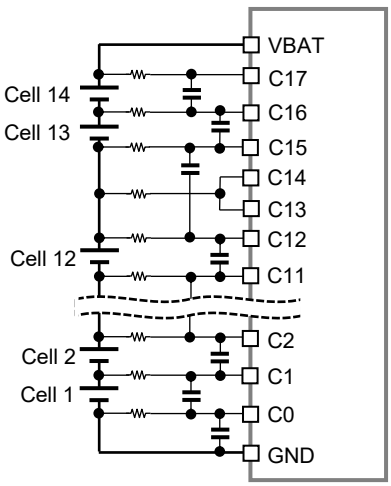


Fig. 5.1.2
Example of
14 Cell System

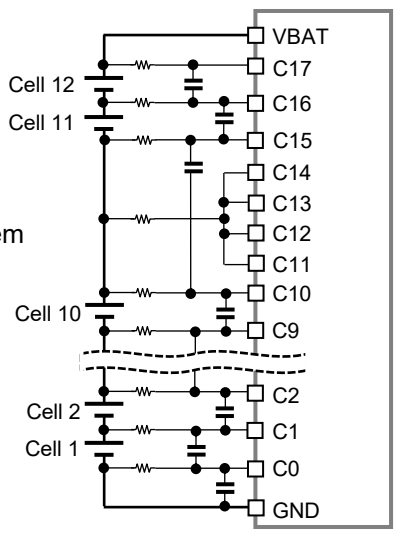


Fig. 5.1.3
Example of
12 Cell System

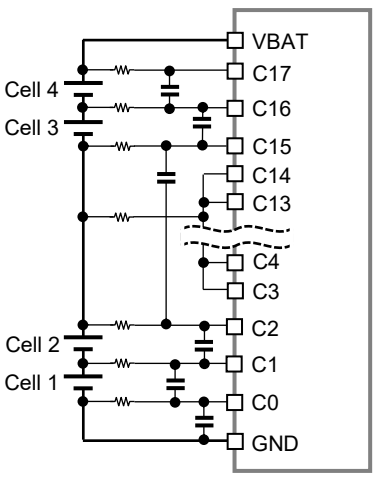


Fig. 5.1.4
Example of
4 Cell System

Chapter 5 Unused pins setting

5.2 Other unused pins:

Table.5.2.1 is a list for unused function pins and its recommended connection method when not used.

Table. 5.2.1 Connection Example for unused function pins

Function	Pin	Connection
Temperature	TMONIn (n=1~6)	Open
Nch FET	CHG, DIS, CP1, CN1	Open
Pch FET	GPIOH1,GPIOH2	Open
Function pin	ALARM1	Open
	FETOFF	Ground
	SHDN	Ground
Current	SRP/SRN	Open or Ground
GPIO	GPIOn (n=1~4)	Open

Chapter 6 Battery Cell inputs connection sequence

6.1 Recommendation

Customer should strongly follow the below recommended Battery Cells connection sequence :

Connect the GND pin first, then followed by VBAT pin.

After that, connect lower cells in turn to upper cells.

GND → VBAT → Cell between C0-C1 → Cell between C1-C2 → Cell between…

6.2 Special case

If the recommended sequence can not be followed, but random connection or partial random connection sequence is required. Please use input resistors bigger than 100ohm for a fully random connection sequence.

For input resistors smaller than 100ohm, connect GND and VBAT first and than random connection for others cell voltage pin.

Note: Connection sequence for special case is verified by simulation with limited numbers of IC test, it seems no risks.

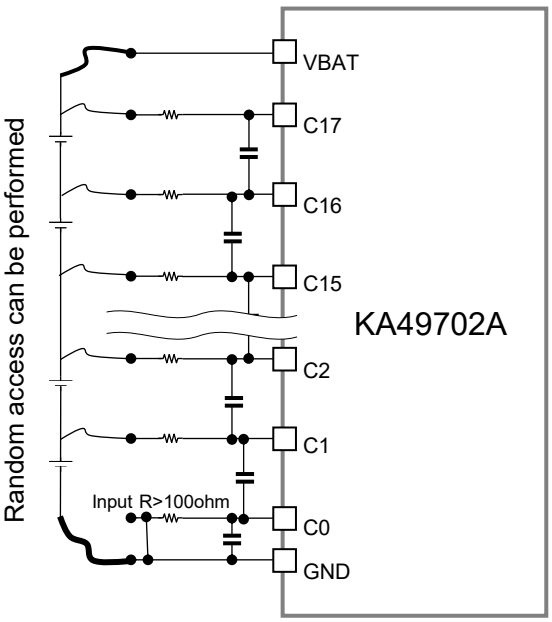


Fig. 6.2.1 Input Resistor bigger than 100ohm

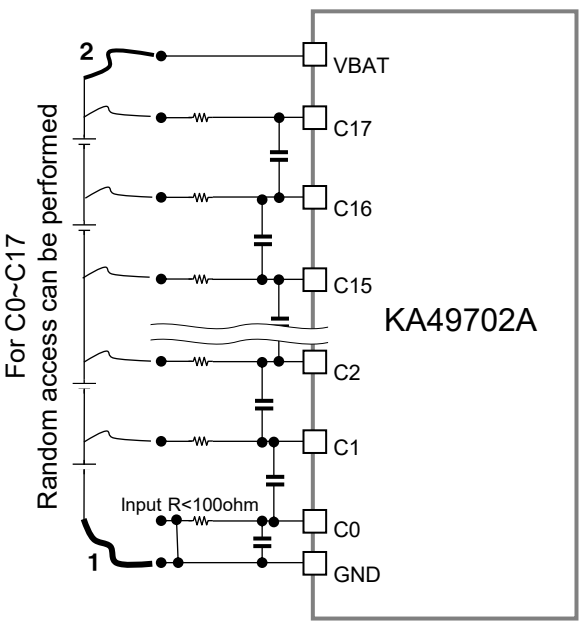


Fig. 6.2.2 Input Resistor smaller than 100ohm

Chapter 7 High-Side FET connection

7.1 Examples for high-side FET connection

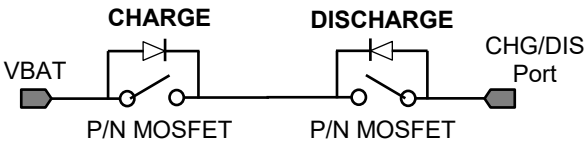


Fig. 7.1.1 Single Port

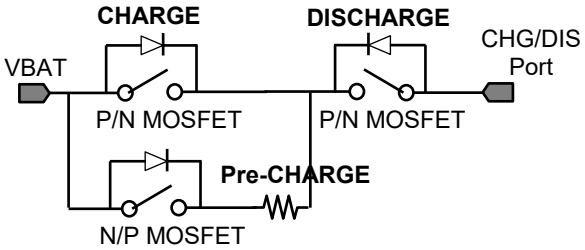


Fig. 7.1.2 Single Port with Pre-charge

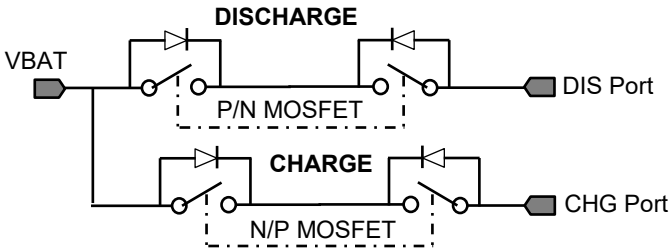


Fig. 7.1.3 Separated port

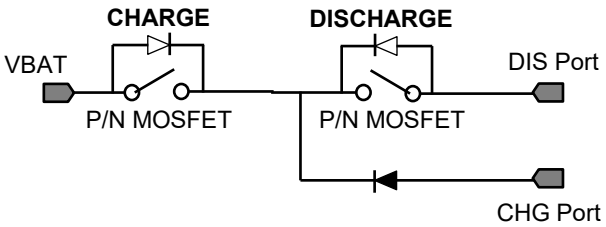


Fig. 7.1.4.a Separated port (Low cost)

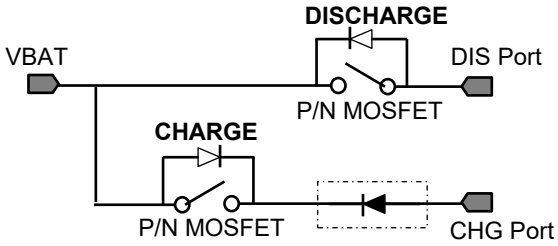


Fig. 7.1.4.b Separated port (Low cost)

7.2 System example for UPS System (Use battery only at emergency)

For certain system such as UPS, the Batteries only need to be used when the external power supply failed. Open or close the FET(Power Loss) by using CHG pin, according to the monitored voltage of External Power by VPACK pin. Make sure the judgement voltage for the switching process is correctly set so that KA49702A to get power from VBAT first before losing External Power. Subsequently, the FET of CHG(P) and DIS(P) can be controlled by GPIOH pins.

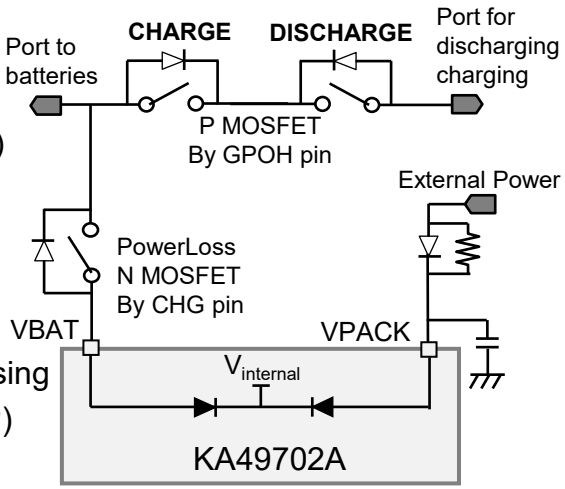


Fig.7.2.1 Switch Power by GPOH

Chapter 8 Low Side FET connection

KA49702 can also be used to drive Low-Side FET by setting FDRV_LOEN (0x04[01]) to “1”. Fig 8.0 shows a typical connection to support Low-Side FET application. Rp limits the current to Zp when CP1 pin is at VBAT voltage, Zp determines the voltage to drive DIS/CHG pin, Dp provides a lower impedance path to drive CHG/DIS pin. Cp is the charging cap to drive Low-Side FET. Additional protection circuits are necessary at CHG pin to cater for wide voltage swing at VPACK- node. This protection circuit causes the CHG FET to be slowly turned off by 10Mohm resistor. By setting GPIO2SEL[3:0] (0x13[11:8]) to “1110”, GPIO2 will output a 50us pulse to enable fast turn off by external circuits, each time CHG FET is disabled.

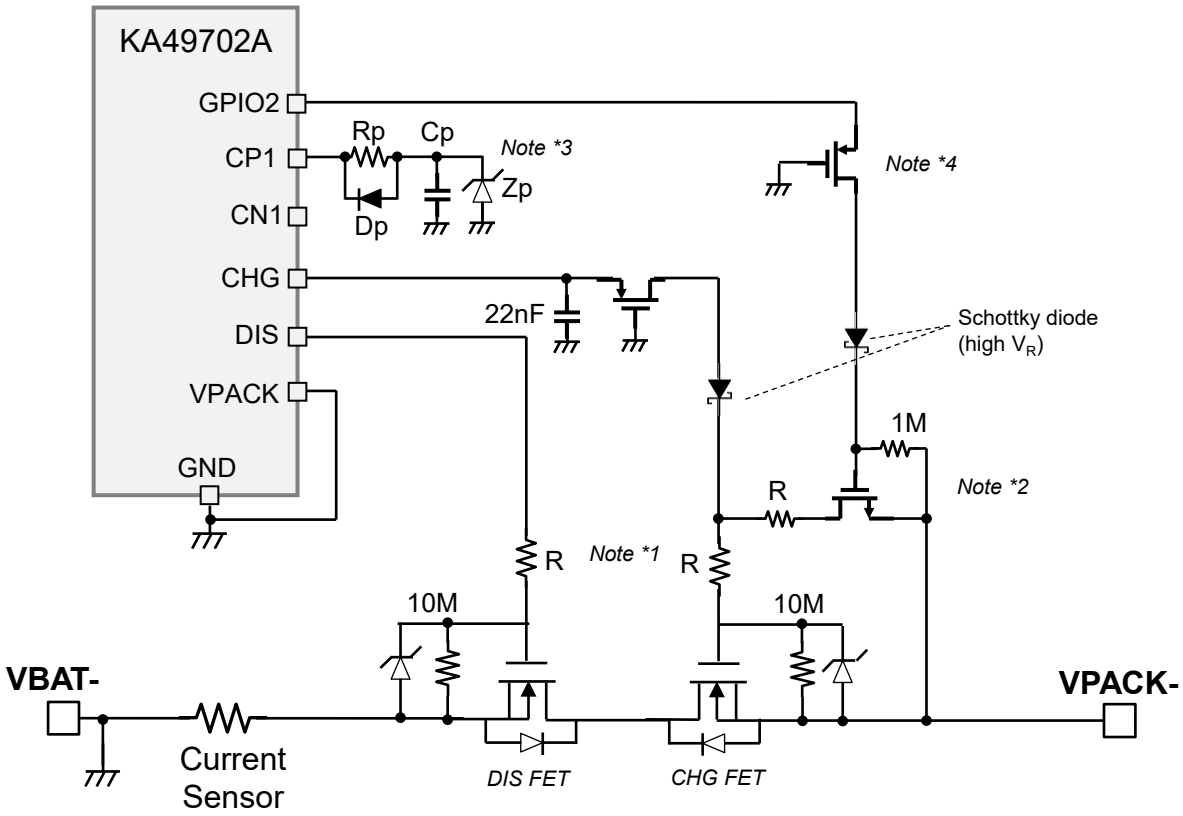


Fig. 8.0 Low-Side FET control circuit with GPIO2 assist

Note :

*1 : The R resistors are to be adjusted based on actual system power FET on/off testing. The common value maybe in tenths or hundreds of ohm.

*2 : More parts are needed for CHG FET control because of VPACK- negative voltage occurrence during Charging.

*3 : Zp is typical Zener diode with Vz =11V.
Dp is typical diode with Vf around 0.6V - 0.8V and high Vr.
$Rp < \frac{(VBATmin - Vz)}{120uA}$

*4 : GPIO2 is set to boost CHG FET turning Off operation.

Below is the alternative Low-Side FETs control system by using the same CHG and DIS pins, without using GPIO2 boost assist.
Set register bit FDRVL_PD (0x25[5]) to “1”.

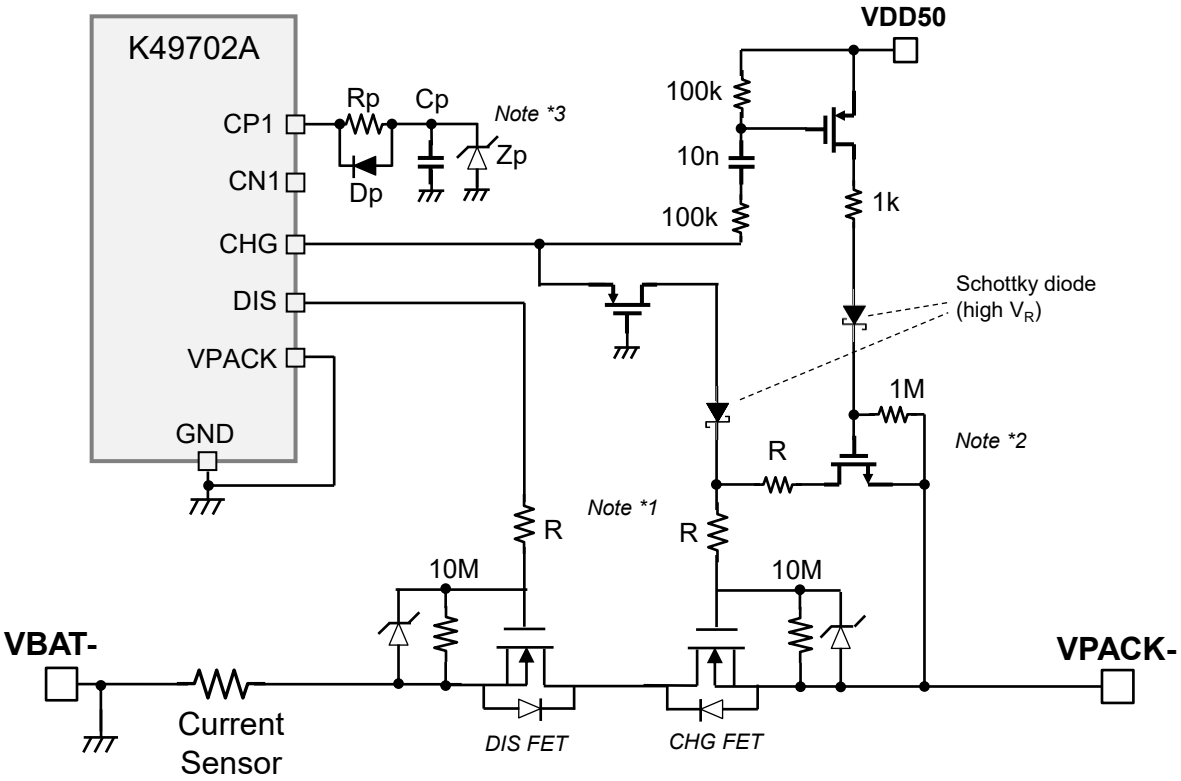


Fig. 8.1 Alternative Low-Side FET control circuit

Note :
*1 : The R resistors are to be adjusted based on actual system power FET on/off testing. The common value is in the range of tenths or hundreds of ohm.
*2 : More parts are needed for CHG FET control because of VPACK- negative voltage occurrence during Charging.
*3 : Zp is typical Zener diode with Vz =11V.
Dp is typical diode with Vf around 0.6V - 0.8V and high Vr.
$Rp < \frac{(VBATmin - Vz)}{120uA}$

In case of system which has external 12V power supply, this supply can be used by CHG and DIS pins internal driver to drive power FETs. Based on the figures shown in Fig 8.0 and Fig 8.1, the circuit can be modified to connect the external 12V supply to CP1 pin as shown in Fig 8.2. In this case, this external 12V becomes the driver supply voltage instead of IC internal charge pump. Set register bit FDRVL_CPOFF (0x25[6]) to “1” to turn off internal charge pump for this operation.

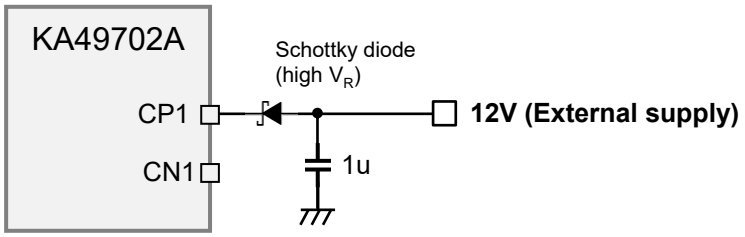


Fig. 8.2 Low-Side FET circuit using external 12V supply

Chapter 9 VPACK,GPIOH1 and GPIOH2 voltage measurement setting

KA49702 can directly measure high voltage with PACK, GPIOH1 and GPIOH2.

For voltage measurement, an attenuator is provided inside the IC, and the configuration is as shown in Figure 9.1. Measurements are affected by the input resistance of external components and the attenuation resistance fluctuations inside the IC, so please take this into account when installing external components.

And, VPACK is used to drive FET Driver and is affected by input current. Use GPIOH1/GPIOH2 when determining measurement accuracy.

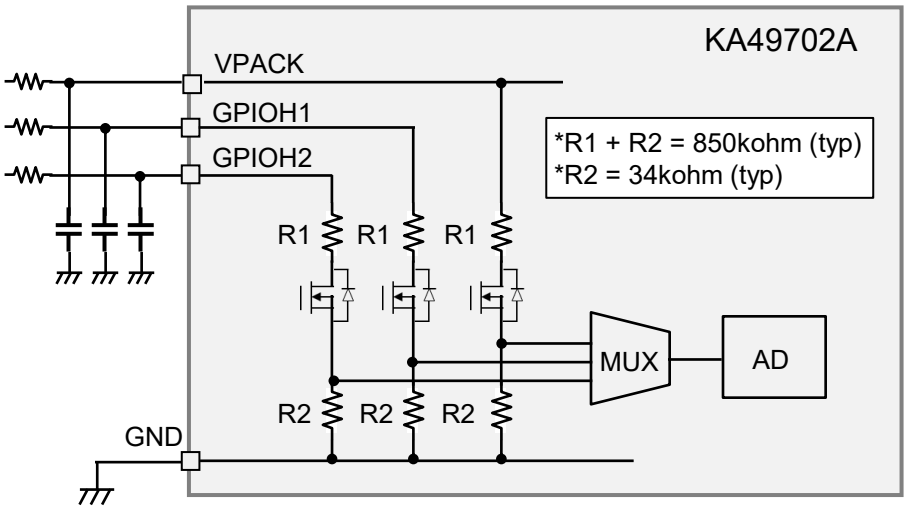


Fig. 9.1 VPACK,GPIOH1 and GPIOH2 voltage measurement circuit

Chapter 10 FET & Fuse Open and Short Detection

KA49702 can detect the abnormality on Charge (CHG) FET, Discharge (DIS) FET and Fuse by using the high voltage VPACK, GPIOH1, GPIOH2 pins and current sensing resistor (Rsense).

For Open and Short circuit detection, the detection points are connected to these pins as shown in below. The failure mode can be judged by the voltage and current measured on these points based on Table in next page.

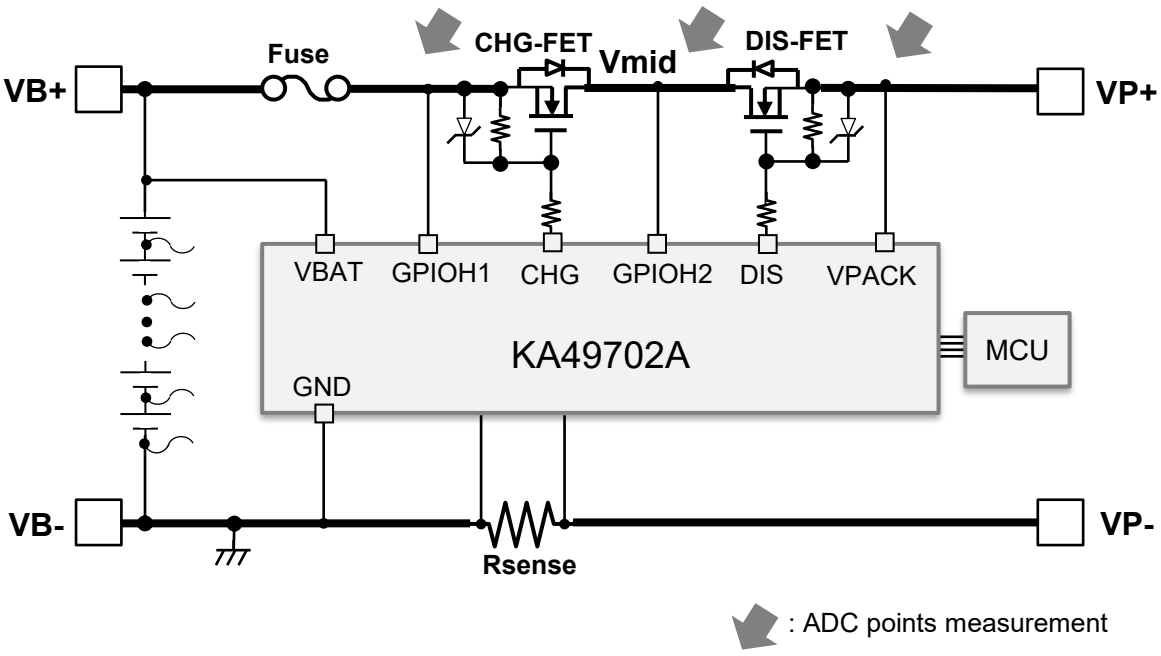


Fig. 10.1 FET & Fuse Open and Short Detection circuit

Chapter 10 FET & Fuse Open and Short Detection

Failure mode	Output condition	MOSFET setting		Checking points (NG = MOSFET/Fuse failure)			
		CHG FET	DIS FET	GPIOH1	GPIOH2 (Vmid)	VPACK (VP+)	Current (Rsense)
CHG-FET Open	Connect Load	ON	ON	Battery voltage	NG: HIZ voltage** OK: battery voltage	NG: HIZ voltage** OK: battery voltage	NG: no current OK: have discharge current
	Connect Charger	ON	ON	Battery voltage	NG: charger voltage* OK: battery voltage	NG: charger voltage* OK: battery voltage	NG: no current OK: have charge current
CHG-FET Short	Connect Load	OFF	ON	Battery voltage	NG: battery voltage OK: Vmid < VB+	NG: battery voltage OK: VP+ < VB+	Have current
	Connect Charger	OFF	ON	Battery voltage	NG: battery voltage OK: charger voltage*	NG: battery voltage OK: charger voltage*	NG: have current OK: no current
DIS-FET Open	Connect Load	ON	ON	Battery voltage	Battery voltage	NG: HIZ voltage** OK: battery voltage	NG: no current OK: have discharge current
	Connect Charger	ON	ON	Battery voltage	Battery voltage	NG: charger voltage* OK: battery voltage	NG: no current OK: have charge current
DIS-FET Short	Connect Load	ON	OFF	Battery voltage	Battery voltage	NG: battery voltage OK: HIZ voltage**	NG: have current OK: no current
	Connect Charger	OFF	OFF	Battery voltage	NG: charger voltage* OK: Vmid < VP+	charger voltage*	No current
Fuse Open	Connect Load	ON	ON	NG: HIZ voltage** OK: battery voltage	NG: HIZ voltage** OK: battery voltage	NG: HIZ voltage** OK: battery voltage	NG: no current OK: have discharge current
	Connect Charger	ON	ON	NG: charger voltage* OK: battery voltage	NG: charger voltage* OK: battery voltage	NG: charger voltage* OK: battery voltage	NG: no current OK: have charge current

*Charger voltage = charger voltage have to be higher than battery voltage in order to differentiate OK and NG condition
**HIZ voltage = HIZ voltage is likely to be pulled low by connected load. This can be differentiated with battery voltage

Table 10.2 Failure mode checking points table

Chapter 11 Watchdog Timer (WDT) setting during MCU firmware updating

Generally, REGEXT pin can be used as a power supply for external MCU, which generates a regulated 3.3V supply. As part of the communication safety features, KA49702A has a Watchdog Timer (WDT) that will countdown to the set time when there is no communication from the MCU, it is possible to shutdown the MCU through shutting down the REGEXT supply. The WDT default time is 60s.

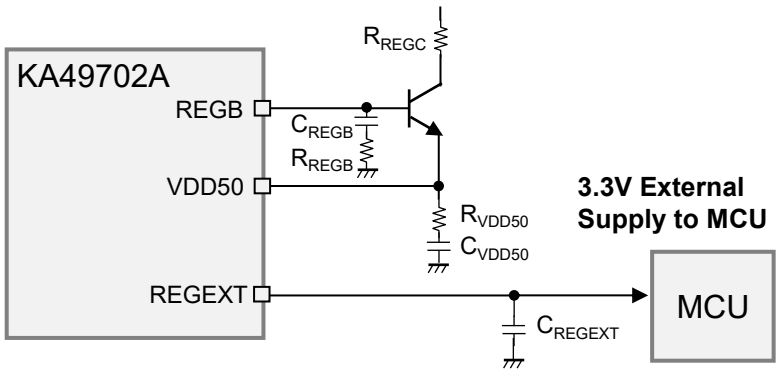


Fig. 11.1 REGEXT supply for MCU

For a particular special usage case, which is during firmware updating on MCU, there is no communication from MCU. This time period may exceed the default WDT. Hence, REGEXT supply will be shutting down and causing failure to the firmware updating process.

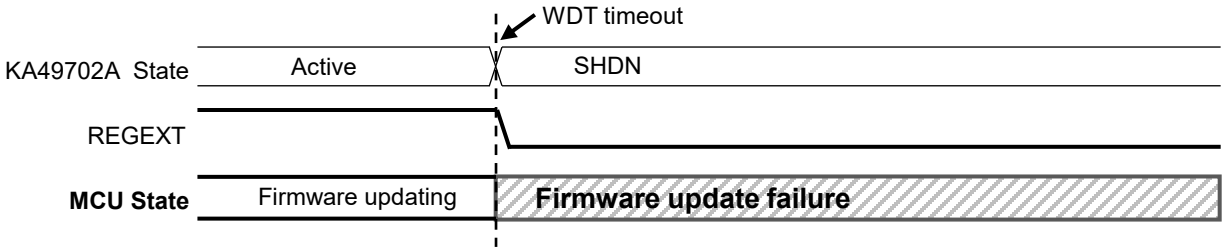


Fig. 11.2 MCU firmware update failure due to WDT timeout

In order to have sufficient time for MCU updating, turn Off WDT or set WDT with longer time before the MCU updating process. (Set register bit COMTIMON (0x03[12]) to “0” or set 1s~4096s for register SPI_WDTCOUNT[11:0] (0x03[11:0])).

After MCU update is completed, turn back On WDT or set back WDT original time.

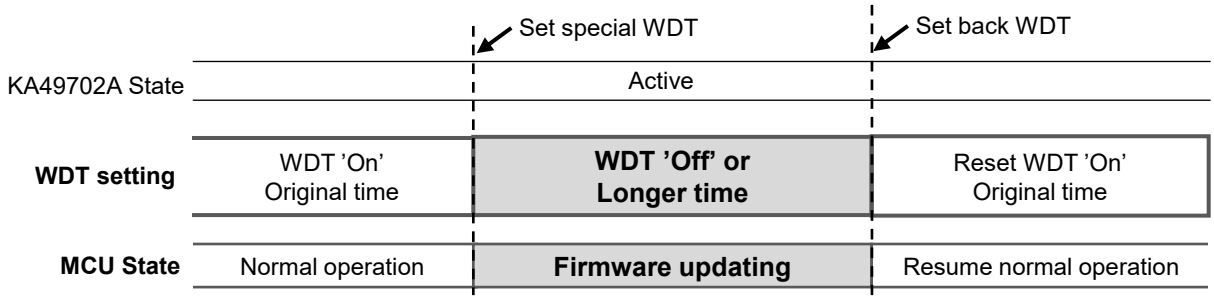
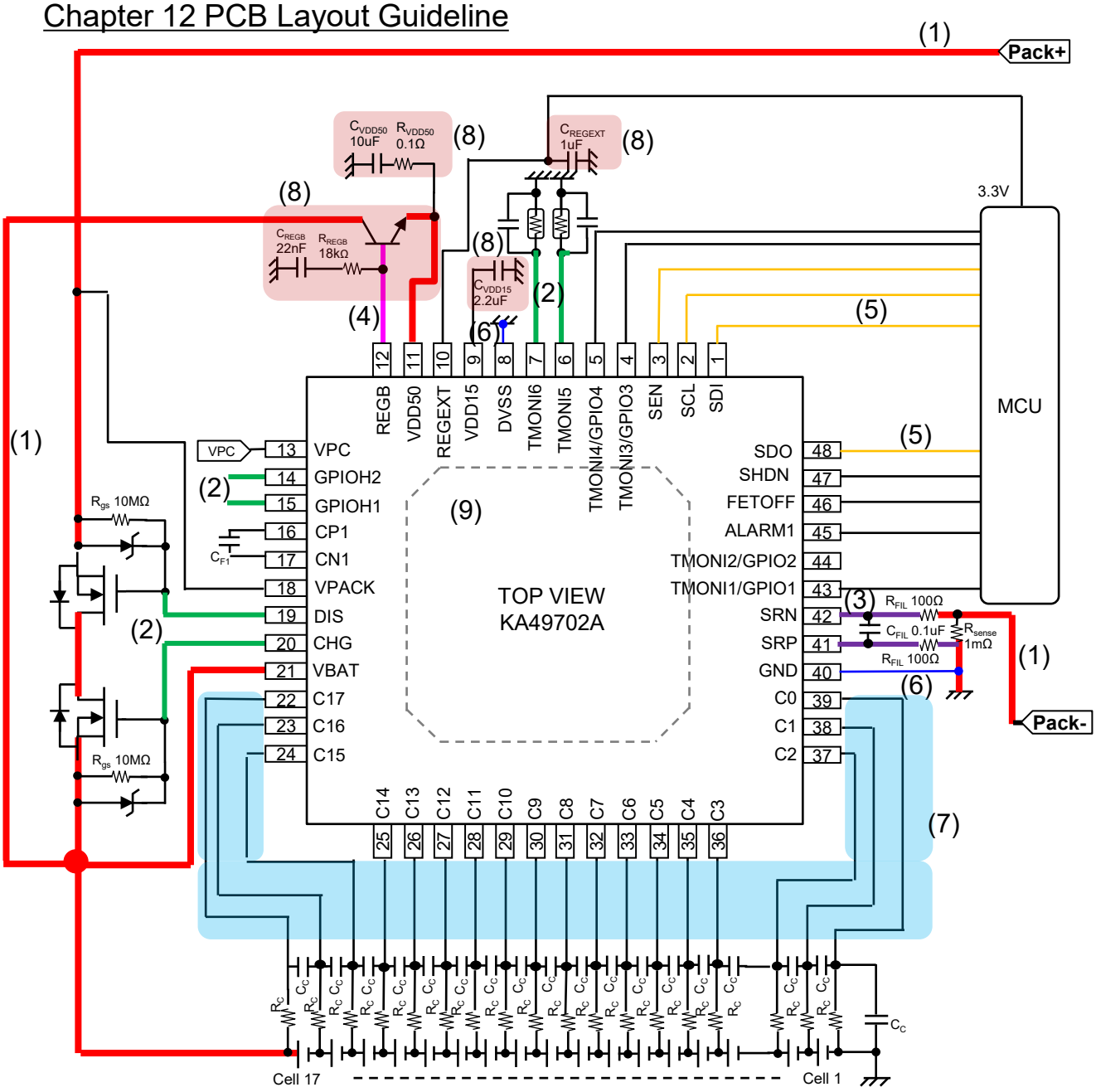


Fig. 11.3 WDT special setting during MCU firmware update

Chapter 12 PCB Layout Guideline



(1) Wide line width to be drawn based on the desired Current.
(2) Away from signals lines. (*for TMONI/GPIO sharing pins, apply only when select TMONI function)
(3) Differential Pair routing which have to be as short as possible and closely identical.
Route both lines on same layer as RC filter. Avoid to be parallel with high current and noisy lines.
For 1 piece Rsense case: Connect both lines directly to the center inner part of Rsense pads.
For multiple Rsense case: All Rsense must be put near together. Connect both lines to the center of this group of Rsense. Evaluate the actual measured current value, adjust the lines connection location or firmware parameter in order to get accurate current reading.
(4) Route lines as short as possible
(5) Insert capacitor if necessary, at communication lines according to your noise test
Draw all the SPI lines as short as possible and with same length to avoid propagation.
Draw all the SPI lines side by side and within the same layer.
Keep noisy lines and high voltage switching lines away from SPI lines.
(6) Connect all ground pins (DVSS, GND) together and routed use copper plane under the IC
(7) Route these lines with the similar shape as much as possible since they are differential signals
(8) Devices to be placed close to IC pin
(9) User can choose to float the bottom heat pad or connect it to GND plane for best heat dissipation

Important Notice

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
   However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board),
   it might be damaged.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins.
   In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.

Revision History

Revision number Rev1.00

Date	Page	Item	Before	After
2024.10.23	—	—	—	First Draft

Revision number Rev1.10

Date	Page	Item	Before	After
2024.11.13	19,20	Low-Side FET control circuit	Connect a capacitor between CP1 and CN1.	Consists of a diode, resistor and capacitor.

Revision number Rev1.20

Date	Page	Item	Before	After
2024.12.04	22,23	Add FET & Fuse Open and Short Detection	NA	Chapter 10: Added application note for FET & Fuse Open and Short Detection using GPIOH1/2 and Vpack pin
	24	Chapter number and relevant figure/table number	Chapter 10 Watchdog Timer (WDT) setting during MCU firmware updating	Chapter 11 Watchdog Timer (WDT) setting during MCU firmware updating
	25	Chapter number	Chapter 11 PCB Layout Guideline	Chapter 12 PCB Layout Guideline
	2	Contents and pages update	Chapter 10 – page 21 Chapter 11 – page 22	Chapter 10 – page 22 Chapter 11 – page 24 Chapter 12 – page 25
2025.2.11	14	Add ESR resistor for VDD15	Fig 4.3.1, 4.3.2 and Table 4.3.3 - No ESR resistor for VDD15	Fig 4.3.1, 4.3.2 and Table 4.3.3 - Add 1Ω ESR resistor for VDD15 in no NPN mode.
2025.2.13	19,20	Low-Side FET control circuit	Fig 8.1, Fig 8.2: CP pin Consists of 2 diode	Fig 8.1, Fig 8.2: CP pin Consists of 1 diode Zp is typical Zener diode with Vz =11V. Dp is typical diode with Vf around 0.6V - 0.8V and high Vr. Rp<((VBATmin −Vz))/120uA
	20	Fig 8.2	--	Schottky diode (high V_R)

Revision number Rev1.30

Date	Page	Item	Before	After
2025.07.09	18	Fig. 7.1.4.b Separated port (Low cost)	Charge to DIS port Discharge to CHG port	Charge to CHG port Discharge to DIS port .
2025.07.15	4	Fig. 2.1.1 and Fig 2.2.1	$\left(MAX(fc)=\left(\frac{fs}{2}\right)=\frac{1}{50us*2}=10KHz\right)$ $eg.when\ fs=20KHz, Rc=1kohm$	$\left(MAX(fc)=\left(\frac{fs}{2}\right)=\frac{1}{50us*2}=10kHz\right)$ $eg.when\ fs=20kHz, Rc=1kohm$

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